

Amendments To The Claims

This listing of claims will replace all previous versions, and listings, of claims in the application.

Listing of claims:

1-44. canceled

45. (currently amended) An electrical circuit comprised of:
at least one dielectric layer comprised of latex; and
at least a corresponding number of layers of electrically conductive material patterned to form multiple electrical interconnects, at least one of the corresponding number of electrically conductive material layers disposed above a corresponding one of the at least one dielectric layer;
wherein one or more of said at least one dielectric layer comprised of latex ~~layers~~ has a top surface that contains peaks and valleys of a size that would not occur on the top surface of the latex had it not been roughened, and one or more of said conductive layers is formed of a first conductive metal that substantially fills said valleys formed in the portion of the latex layer's top surface over which the conductive layer's metal has been patterned, so as to increase the ability of said metal to adhere to said latex surface.
46. (original) A circuit as in Claim 45 wherein the portions of said one or more layers of the first conductive metal adjacent said latex layer between said peaks and valleys contain particles of a second metal that were used as catalytic seed particles to promote the deposition of said first metal onto the roughened top surface of said latex layer.
47. (original) A circuit as in Claim 46 wherein a majority of the catalytic seed particles contained in said first conductive metal adjacent the top surface of said latex layer contain only two to six atoms of said second metal.
48. (original) A circuit as in Claim 46 wherein the second metal of which said catalytic seed particles are formed is a metal in the eighth group of the periodic table.

49. (original) A circuit as in Claim 46 wherein said second metal is palladium.
50. (currently amended) A multichip module comprising:
a plurality of integrated circuits mounted on a substrate;
at least one flexible dielectric layer comprised of latex; and
at least a corresponding number of layers of electrically conductive material
patterned to form multiple electrical interconnects between bonding pads on different
ones of said integrated circuits, at least one of the corresponding number of electrically
conductive material layers disposed above a corresponding one of the at least one flexible
dielectric layer;-
wherein one or more of said at least one flexible dielectric layer comprised of
latex ~~layers~~ has a top surface that contains peaks and valleys of a size that would not
occur on the top surface of the latex had it not been roughened, and one or more of said
conductive layers is formed of a first conductive metal that substantially fills said valleys
formed in the portion of the latex layer's top surface over which the conductive layer's
metal has been patterned, so as to increase the ability of said metal to adhere to said latex
surface.
51. (original) A multichip module as in Claim 50 wherein the portions of said one or more
layers of the first conductive metal adjacent said latex layer between said peaks and
valleys contain particles of a second metal that were used as catalytic seed particles to
promote the deposition of said first metal onto the roughened top surface of said latex
layer.
52. (original) A multichip module as in Claim 51 wherein a majority of the catalytic seed
particles contained in said first conductive metal adjacent the top surface of said latex
layer contain only two to six atoms of said second metal.

53. (original) A multichip module as in Claim 51 wherein the second metal of which said catalytic seed particles are formed is a metal in the eighth group of the periodic table.

54. (original) A multichip module as in Claim 52 wherein said second metal is palladium.